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Description

[THIN FILM TRANSISTOR ARRAY AND FABRICATING METHOD THEREOF]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority benefit of Taiwan application serial no. 93111981, filed April 29, 2004.

BACKGROUND OF INVENTION

[0002] Field of Invention

[0003] The present invention relates to a thin film transistor array (TFT array) and a fabricating method thereof. More particularly, the present invention relates to a thin film transistor array (TFT array) having an enhanced storage capacitor and a fabricating method thereof.

[0004] Description of Related Art

[0005] The proliferation of multi-media systems in our society depends to a large extent on the progressive development of semiconductor devices and display devices. Display devices such as the cathode ray tube (CRT) have been used

for quite some time due to its remarkable display quality, reliability and low cost. Although the conventional CRT has many advantages, but the design problem of the electron gun renders is heavy, bulky and energy wasting. Moreover, there is always some potential danger of hurting viewer's eyes due to its emission of some radiation. With big leaps in the techniques of manufacturing semiconductor devices and optic-electronics devices, high picture quality, slim, low power consumption and radiation-free displays such as the thin film transistor liquid crystal displays (TFT-LCD) have gradually become mainstream display products.

[0006] Generally, a color TFT-LCD includes a color filter (C/F), a TFT array and a liquid crystal layer disposed therebetween. The TFT array includes a plurality of thin film transistors, which is arranged in an area array and is driven by a plurality of scan lines and data lines. Each thin film transistor is disposed in a pixel area and is electrically connected to a corresponding pixel electrode formed by indium tin oxide (ITO), indium zinc oxide (IZO) or other transparent conductive materials. Each thin film transistor is used to drive the liquid crystal layer to show various gray levels. Furthermore, in a pixel of the conventional

TFT array, a storage capacitor may be formed by a pixel electrode, the corresponding scan line and a dielectric layer (e.g. a gate insulator and/or a passivation layer) therebetween. Also, the storage capacitor can be formed by a pixel electrode, a common line and a dielectric layer therebetween to provide better picture quality. In the prior art, storage capacitor is classified into Metal-Insulator-Metal (MIM) type and Metal-Insulator-ITO (MII) type, which are described as follow.

[0007] FIG. 1 is a cross-sectional view of a conventional MIM type storage capacitor. Referring to FIG. 1, in a conventional pixel structure, a MIM type storage capacitor is coupled by a scan line (not shown) and an upper electrode 120 or is coupled by a common line 100 and an upper electrode 120. It should be noted that the common line 100 (or the scan line) and the upper electrode is electrical isolated by a gate insulator 110 therebetween in the MIM type storage capacitor. Therefore, capacitance of the MIM type storage capacitor relates to thickness of the gate insulator 110. In other words, the smaller the thickness of the gate insulator 110, the larger the capacitance Cst of the MIM type storage capacitor is. Furthermore, a pixel electrode 140 is electrically connected to the upper electrode 120 through

a contact via 132 formed in a passivation layer 130.

[0008] FIG. 2 is a cross-sectional view of a conventional MII type storage capacitor. Referring to FIG. 2, in a conventional pixel structure, a MII type storage capacitor is coupled by a scan line (not shown) and a pixel electrode 230 or is coupled by a common line 200 and a pixel electrode 230. Compared with the MIM type storage capacitor, the common line 200 (or the scan line) and the pixel electrode 230 is electrical isolated by a gate insulator 210 and a passivation layer 220 therebetween in the MII type storage capacitor. Therefore, capacitance of the MII type storage capacitor relates to total thickness of the gate insulator 210 and the passivation layer 220. In other words, the smaller the total thickness of the gate insulator 210 and the passivation layer 220, the larger the capacitance Cst of the MIM type storage capacitor is.

[0009] In the conventional TFT array mentioned above, the thickness of the gate insulator 210 and/or passivation layer 220 must be reduced to obtain a larger capacitance Cst without lowering aperture ratio. However, the reliability of thin film transistors may be affected when the thickness of the gate insulator 210 and/or passivation layer 220 is reduced.

SUMMARY OF INVENTION

[0010] The invention provides a thin film transistor array to increase the capacitance of the storage capacitor of each pixel.

[0011] The invention provides a fabricating method of a thin film transistor array, which is compatible with current processes, to increase the capacitance of the storage capacitor of each pixel.

[0012] According to an embodied of the present invention, the thin film transistor array including a substrate, a plurality of scan lines, a plurality of data lines, a plurality of thin film transistor, an etching stop layer and a plurality of pixel electrodes is provided. The scan lines and the data lines are disposed over the substrate and the substrate is defined into a plurality of pixel areas by the scan lines and the data lines. Each thin film transistor is disposed in one of the pixel areas and is driven by the scan lines and the data lines correspondingly. The etching stop layer is disposed over the scan lines, and the etching stop layer has a plurality of openings. Each pixel electrode is disposed in one of the pixel areas and is electrically connected to one of the thin film transistors correspondingly, wherein a portion of each pixel electrode is coupled toone of the

scan lines through one of the openings to form a storage capacitor.

[0013] According to an embodied of the present invention, the thin film transistor array including a substrate, a plurality of scan lines, a plurality of data lines, a plurality of thin film transistor, a plurality of common lines, an etching stop layer and a plurality of pixel electrodes is provided. The scan lines and the data lines are disposed over the substrate and the substrate is defined into a plurality of pixel areas by the scan lines and the data lines. Each thin film transistor is disposed in one of the pixel areas and is driven by the scan lines and the data lines correspondingly. The common lines are disposed over the substrate, wherein each common line is located between two adjacent scan lines. The etching stop layer is disposed over the common lines, wherein the etching stop layer has a plurality of openings. Each pixel electrode is disposed in one of the pixel areas and is electrically connected to one of the thin film transistors correspondingly, wherein a portion of each pixel electrode is coupled toone of the scan lines through one of the openings to form a storage capacitor.

[0014] In an embodiment of the present invention, the thin film

transistor array further including a gate insulator disposed between the etching stop layer and the scan lines (or the common lines). Furthermore, the gate insulator has a plurality of recesses, and each recess is located under one of the openings of the etching stop layer.

[0015] In an embodiment of the present invention, the thin film transistor array further including a semiconductor layer disposed between the etching stop layer and the gate insulator. Moreover, the thin film transistor array further including a passivation layer disposed over the etching stop layer and the gate insulator, wherein the openings of the etching stop layer is exposed by the passivation.

[0016] In an embodiment of the present invention, the etching stop layer includes a plurality of stripe patterns; each stripe pattern is located above one of the scan lines (or common lines) correspondingly. Furthermore, the etching stop layer includes a plurality of frame patterns; each frame pattern is located under one of the pixel electrodes correspondingly.

[0017] In an embodiment of the present invention, a material of the pixel electrodes comprises ITO, IZO or other transparent conductive material.

[0018] According to an embodied of the present invention, the

fabricating method of a thin film transistor array is provided. First, a first patterned conductive layer is formed over the substrate, and then a gate insulator and a semiconductor material layer is formed over the substrate and the first patterned conductive layer sequentially. Thereafter, an etching stop layer located above the first patterned conductive layer is formed over a portion of the semiconductor material layer. Next, a second conductive material layer is formed over the semiconductor material layer and the etching stop layer. Afterward, the second conductive material layer and the semiconductor material layer are patterned to simultaneously form a second patterned conductive layer and a plurality of semiconductor layers, which are located under the etching stop layer and the second patterned conductive layer. Then, a passivation layer is formed over the substrate, and a portion of the passivation layer, which is located on the second patterned conductive layer, is removed to form a plurality of contact windows. At the same time, a portion of the passivation layer, the etching stop layer and the semiconductor layers, which are located above the first patterned conductive layer, are removed simultaneously. Ultimately, a plurality of pixel electrodes is formed over the sub-

strate. Wherein each pixel electrode is electrically connected to the second patterned conductive layer through one of the contact windows, and a portion of each pixel electrode is coupled to the first patterned conductive layer through one of the openings to form a storage capacitor.

[0019] In an embodiment of the present invention, the fabricating method further includes forming an ohmic contact layer over the semiconductor material layer and the etching stop layer before forming the second conductive material layer over the semiconductor material layer and the etching stop layer.

[0020] In an embodiment of the present invention, the first patterned conductive layer is formed by forming a first conductive material layer over the substrate, and then the first conductive material layer is patterned to form a plurality of scan lines and a plurality of gates connected with the scan lines. Furthermore, the etching stop layer is formed above the gates and the scan lines.

[0021] In an embodiment of the present invention, the first patterned conductive layer is formed by forming a first conductive material layer over the substrate. And then the first conductive material layer is patterned to form a plurality of scan lines, a plurality of gates connected with the

scan lines and a plurality of common lines located between two adjacent scan lines. Furthermore, the etching stop layer is formed above the gates and the common lines.

[0022] In an embodiment of the present invention, the fabricating method further includes removing partial thickness of the etching stop layer by using the second patterned conductive layer as a mask during patterning the second conductive material layer and the semiconductor material layer.

[0023] In an embodiment of the present invention, the fabricating method further includes removing partial thickness of the gate insulator to form a plurality of recesses, which are located under the openings, when forming the contact windows.

[0024] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF DRAWINGS

[0025] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, to-

gether with the description, serve to explain the principles of the invention.

[0026] FIG. 1 is a cross-sectional view of a conventional MIM type storage capacitor.

[0027] FIG. 2 is a cross-sectional view of conventional MII type storage capacitor.

[0028] FIG. 3 is a top view of the thin film transistor array according to an embodiment of the present invention.

[0029] FIG. 4A is a top view of the etching stop layer according to an embodiment of the present invention.

[0030] FIG. 4B is a top view of the etching stop layer according to another embodiment of the present invention.

[0031] FIG. 5 is a cross-sectional view of the thin film transistor array according to another embodiment of the present invention.

[0032] FIG. 6A through FIG. 6H is the fabricating process of the thin film transistor array according to one embodiment of the present invention.

DETAILED DESCRIPTION

[0033] FIG. 3 is a top view of the thin film transistor array according to an embodiment of the present invention. Referring to FIG. 3, the thin film transistor array 300 of the present invention includes a substrate 310, a plurality of

scan lines 320, a plurality of data lines 330, a plurality of thin film transistor 340, an etching stop layer 350 and a plurality of pixel electrodes 360.

[0034] In an embodiment of the present invention, the substrate 310 includes a glass substrate, a plastic substrate or substrate made of by other material. As shown in FIG. 3, the scan lines 320 and the data lines 330 are disposed over the substrate 310, which is defined into a plurality of pixel areas 312 by the scan lines 320 and the data lines 330. More specifically, the scan lines 320 are arranged parallel to each other over the substrate 310, and the data lines 330 arranged parallel to each other over the substrate 310, for example. Since the extended direction of the scan lines 320 is perpendicular to the extended direction of the data lines 330, the substrate 310 is defined into rectangular pixel areas 312.

[0035] Each thin film transistor 340 is disposed in one of the pixel areas 312 and is driven by the scan lines 320 and the data lines 330 correspondingly. More specifically, the thin film transistor 340 is disposed adjacent to the intersection of the scan line 320 and the data line 330, i.e. the thin film transistor 340 is disposed at a corner of the pixel area 312. In an embodiment of the present invention, the

thin film transistor 340 includes a gate 342, a semiconductor layer 344 located above the gate 342, and a source/drain 346, for example. Wherein the gate 342 and the scan line 320 may be formed simultaneously, and the source/drain 346 and the data line 330 may be formed simultaneously.

[0036] Referring to FIG. 3, the etching stop layer 350 is disposed over the scan lines 320, and the etching stop layer 350 has a plurality of openings 352 (referring to FIG. 4A and 4B). Furthermore, each pixel electrode 360 is disposed in one of the pixel areas 312 and is electrically connected to one of the thin film transistors 340 correspondingly. Wherein a portion of each pixel electrode 360 is coupled toone of the scan lines 320 through one of the openings 352 to form a storage capacitor. The storage capacitor is a MII type storage capacitor and the cross-sectional view thereof is shown in FIG. 6A through FIG. 6H. As described above, the material of the pixel electrode 360 includes indium tin oxide (ITO), indium zinc oxide (IZO) or other transparent conductive material.

[0037] FIG. 4A is a top view of the etching stop layer according to an embodiment of the present invention; and FIG. 4B is a top view of the etching stop layer according to another

embodiment of the present invention. Referring to FIG. 4A, in accordance with one embodiment of the present invention, the etching stop layer 350 includes a plurality of stripe patterns 350a having openings 352, each stripe pattern 350a is located above one of the scan lines 320 correspondingly. Referring to FIG. 4A, in accordance with another embodiment of the present invention, the etching stop layer 350 includes a plurality of frame patterns 350b; each frame pattern 350b is located under one of the pixel electrodes 360 correspondingly.

[0038] FIG. 5 is a cross-sectional view of the thin film transistor array according to another embodiment of the present invention. Referring FIG. 5, the thin film transistor array 300' of the present invention includes a substrate 310, a plurality of scan lines 320, a plurality of data lines 330, a plurality of thin film transistor 340, a plurality of common lines 370, an etching stop layer 350 and a plurality of pixel electrodes 360. Since the thin film transistor array 300' are similar to the thin film transistor array 300 shown in FIG. 3, only difference between the thin film transistor array 300' and the thin film transistor array 300 is described.

[0039] Referring to FIG. 6, the common line 370 is disposed be-

tween two adjacent scan lines 320. It should be noted that the common line 370 and the scan lines 320 could be formed simultaneously. Since the storage capacitor of the thin film transistor array 300' is formed over the common lines 370, the etching stop layer 350 is disposed above the common lines 370. Similarly, the etching stop layer 350 described in this embodiment has a plurality of openings 352, so that a portion of each pixel electrode 360 is coupled toone of the common lines370 through one of the openings 352 to form a storage capacitor. The cross-sectional viewthe storage capacitor is shown in FIG. 6A through FIG. 6H.

[0040] FIG. 6A through FIG. 6H is the fabricating process of the thin film transistor array according to one embodiment of the present invention. Referring to FIG. 6A, first, a first patterned conductive layer M1 is formed over the substrate 310, and the first patterned conductive layer M1 includes aluminum (Al) or other conductive material.

[0041] When fabricating the thin film transistor array 300 (shown in FIG. 3) having a Cst on gate structure, the first patterned conductive layer M1 is formed by forming a first conductive material layer (not shown) over the substrate 310, and then the first conductive material layer is pat-

terned to form a plurality of scan lines 320 and a plurality of gates 342, which are electrically connected with the scan lines 320 correspondingly.

[0042] When fabricating the thin film transistor array 300' (shown in FIG. 5) having a Cst on common structure, the first patterned conductive layer M1 is formed by forming a first conductive material layer (not shown) over the substrate 310, and then the first conductive material layer is patterned to form a plurality of scan lines 320, and a plurality of gates 342 connected with the scan lines 320, and a plurality of common lines 370 located between two adjacent scan lines 320.

[0043] Then, referring to FIG. 6B, a gate insulator 380 and a semiconductor material layer 344' is formed over the substrate 310 and the first patterned conductive layer M1 sequentially. Wherein the gate insulator 380 includes silicon oxide, silicon nitride or other dielectric material, and the semiconductor material layer 344' includes amorphous silicon, for example.

[0044] Referring to FIG. 6C, an etching stop layer 350 located above the first patterned conductive layer M1 is formed over a portion of the semiconductor material layer 344'. It should be noted that the etching stop layer 350 is formed

above the gates 342 and the scan lines 320, when fabricating the thin film transistor array 300 (shown in FIG. 3) having a Cst on gate structure. Furthermore, the etching stop layer 350 is formed above the gates 342 and the common lines 370, when fabricating the thin film transistor array 300' (shown in FIG. 5) having a Cst on common structure.

[0045] Referring to FIG. 6D, a second conductive material layer 382 is formed over the semiconductor material layer 344'and the etching stop layer 350. The second conductive material layer 382 is, for example, an aluminum / molybdenum / aluminum (Al / Mo / Al) stacked layer, a single metal layer or a composite metal layer. In order to enhance the performance of the devices, an ohmic contact layer 384 could be formed over the semiconductor material layer 344' and the etching stop layer 350 before forming the second conductive material layer 382. Therefore, the adhesion between second conductive material layer 382 and the semiconductor material layer 344'could be enhanced. As described above, the ohmic contact layer 384 is, for example, an n-type doped amorphous silicon.

[0046] Referring to FIG. 6E, the second conductive material layer 382, the ohmic contact layer 384 and the semiconductor

material layer 344' are patterned to simultaneously form a second patterned conductive layer M2 and a plurality of semiconductor layers 344, which are located under the etching stop layer 350 and the second patterned conductive layer M2. After the patterning process, the ohmic contact layer 384 is only located under the second patterned conductive layer M2. In other words, the pattern of the ohmic contact layer 384 and the second patterned conductive layer M2 are the same.

[0047] Referring to FIG. 6E, partial thickness of the etching stop layer 350 is removed, by using the second patterned conductive layer M2 as a mask during patterning the second conductive material layer M2 and the semiconductor material layer 344'. Wherein the profile of the etching stop layer 350 before etching is shown as A and B of FIG. 6E.

[0048] Referring to FIG. 6F and FIG. 6G, a passivation layer 390 is formed over the substrate 310, and then a portion of the passivation layer 390, which is located on the second patterned conductive layer M2, is removed to form a plurality of contact windows 392. At the same time, a portion of the passivation layer 390, the etching stop layer 350 and the semiconductor layers 344, which are located above the first patterned conductive layer M1, are removed si-

multaneously to form a plurality of openings 394. In this embodiment, the contact windows 392 and the openings 394 are, for example, formed by performing a photolithography/etch process. After performing the photolithography/etch process, a portion of the second patterned conductive layer M2 is exposed by the contact windows 392, and a portion of the gate insulator 380 is exposed by the openings 394. Furthermore, partial thickness of the gate insulator 380 may be removed to form a plurality of recesses R, which are located under the openings, when forming the contact windows 392. Instead of openings, the recesses R is formed in the gate insulator 380 because of the etching stop layer 350.

[0049] Referring to FIG. 6H, ultimately, a plurality of pixel electrodes 360 is formed over the substrate 310. Wherein each pixel electrode 360 is electrically connected to the second patterned conductive layer M2 through one of the contact windows 392, and a portion of each pixel electrode 360 is coupled to the first patterned conductive layerM1 through one of the openings 394 to form a storage capacitor. It should be noted that the recesses R formed on a surface of the gate insulator 380 reduce the thickness thereof; therefore the capacitance of the storage ca-

pacitor can be increased.

[0050] As described above, the present invention at least provides the following advantages:

[0051] 1. In the thin film transistor array of the present invention, the capacitance of the storage capacitor and aperture ratio thereof is increased.

[0052] 2. The fabricating method of the thin film transistor array is compatible with current processes. More specifically, the capacitance of the storage capacitor is significantly increased without modifying processes substantially.

[0053] The foregoing description of the preferred embodiment of the present invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form or to exemplary embodiments disclosed. Accordingly, the foregoing description should be regarded as illustrative rather than restrictive. Obviously, many modifications and variations will be apparent to practitioners skilled in this art. The embodiments are chosen and described in order to best explain the principles of the invention and its best mode practical application, thereby to enable persons skilled in the art to understand the invention for various embodiments and with various modifications as are suited

to the particular use or implementation contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents in which all terms are meant in their broadest reasonable sense unless otherwise indicated. It should be appreciated that variations may be made in the embodiments described by persons skilled in the art without departing from the scope of the present invention as defined by the following claims. Moreover, no element and component in the present disclosure is intended to be dedicated to the public regardless of whether the element or component is explicitly recited in the following claims.